Electronic Version
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Claims

[c1] 1. A method comprising the steps of:

identifying element density of at least one functional circuit block;

identifying element attributes of elements associated with the at least one functional circuit block;

forming an element density function parameterized from the element attributes; and

modifying placement of the at least one functional circuit block relative to other functional circuit blocks based on the element density function to substantially eliminate latching effects in a circuit.

[c2] 2.The method of claim 1, wherein the element density is at least one of PFET density and NFET density.

[c3] 3. The method of claim 2, wherein the modifying placement step includes:

placing the NFET density of a given functional circuit block away from a source of undershoot; and

placing the PFET density of a given functional circuit block away from a source of overshoot.

[c4] 4. The method of claim 1, wherein the step of identifying

element attributes includes identifying at least one of sensitive to temperature, power, overshoot, undershoot, external sources, injection mechanisms, element pair density and strength and latchup resiliency, orientation and form factor in the at least one functional circuit block and spatial density.

[c5] 5. The method of claim 1, further comprising providing decoupling capacitor elements to fill space or add capacitance to eliminate propagation adjacent an injection source to avoid propagation of latchup or soft latchup.

[c6] 6. The method of claim 1, wherein prior to the modifying placement step, the method further comprising the steps of determining at least one of:

(i) orientation and placement of an injecting source;

(ii) distance between an ESD element and adjacent region of high pnpn density;

(iii) form factors of the at least one functional circuit block;

(iv) guard ring utilization between adjacent functional circuit blocks;

(v) NPN density - Number of npn per unit area;

(vi) NPN parameter strength (current gain);

(vii) PNP density - Number of pnp per unit area;

(viii) PNP parameter strength (pnp current gain);

(ix) parameterization of the NPN density as a function

of strength parameters statistics;

(x) parameterization of the PNP density as a function of the strength parameters statistics;

(xi) PNPN density; and

(xii)PNPN parameter strength.

[c7] 7. The method of claim 1, wherein identifying element density of the at least one functional circuit block includes identifying element density at a perimeter of the at least one functional circuit block to determine a surface density function on the perimeter.

[c8] 8. The method of claim 1, wherein the modifying placement step includes spacing the at least one functional circuit block apart from the other functional circuit blocks to reduce coupling strength between elements associated therewith.

[c9] 9. The method of claim 1, further comprising the step of determining magnitude of latchup sensitivity of a specific circuit by:

$$F = \beta_{npn}\beta_{pnp} / [(I_{DD} + I_{RW}\beta_{npn}) / (I_{DD} - I_{RW} - I_{RS}(\beta_{npn}+1)/(\beta_{npn}))]$$

wherein when (i) F is less than 1, then latchup does not occur and (ii) F > 1 then latchup will occur.

[c10] 10. The method of claim 1, wherein the element density

function includes:

counting independent BP shapes indicating a number of pnp elements thereby determining a number of p diffusions associated with the at least one functional circuit block; and

counting of independent ROX shapes indicating the number of npn elements associated with the at least one functional circuit block.

[c11] 11. The method of claim 10, further comprising determining a number of pnpn and npnp elements based on the number of npn elements and pnp elements to determine element density of the at least one functional circuit block.

[c12] 12. The method of claim 9, wherein:

a relative distance between a location of an injecting source and a collecting circuit at (i) comprising elements associated with the at least one functional circuit block is designated as a vector R r_i, where an injector is at a vector position R and a collecting structure is at vector position r_i;

a relative distance between the location of a first circuit at (i) and a second circuit (j) of the at least one functional circuit block is designated as a vector r_i r_j;

a spatial function is established which is a relative strength of injection source at R at the position (i);

and

wherein a function is created where:

(i) if an N_{pnpn} ($F > 1$) of a first chip region is greater than the N_{pnpn} ($F > 1$) of a second chip region then the first chip region is moved farther away from the injection region;

(ii) if the N_{pnpn} ($F < 1$) of the first chip region is greater than the N_{pnpn} ($F < 1$) of the second chip region then the first chip region is moved closer to the injection region; and

(iii) if the N_{pnpn} (F) = 0 for the first chip region, then the first chip region is move closest to the injection region.

[c13] 13. The method of claim 12, wherein an injection current strength is defined as:

$$I_{injection} = [I_{inj} (R)) / | R - r_i |^2] \exp - \{ | R - r_i | / (D \tau)^{1/2}) \}$$

where I injection = I_{RW},

wherein when the at least one functional circuit block contains elements whose initial state is $F > 1$ after placement of the functional circuit block,

the method further includes the steps of:

performing a re-optimization of local elements by changing spacing of well contact and substrate

contacts associated with the elements.

[c14] 14. The method of claim 12, wherein placement is chosen based on peak temperature at location R.

[c15] 15. A method comprising the steps of:
identifying element attributes within a functional circuit block;
forming an element density function parameterized from the element attributes; and
placing the functional circuit block based on the element density function to substantially eliminate latching effects in a circuit.

[c16] 16. A method, as recited in claim 15, wherein the element density is a parasitic transistor structure.

[c17] 17. A method, as recited in claim 15, wherein the element density function includes the element attributes relevant to latchup.

[c18] 18. A method, as recited in claim 15, wherein the placement of the functional circuit block is based on the position relative to a injection stimulus.

[c19] 19. A method, as recited in claim 15, further comprising identifying further functional circuit blocks, the function circuit block and the further function circuit blocks in-

clude at least one of:

(i) peripheral circuits;

(ii) ESD networks;

(iii) ESD Power clamps;

(iv) decoupling Capacitors;

(v) DRAM array;

(vi) SRAM array;

(vii) gate array; and

(viii) CMOS logic.

[c20] 20. A method as recited in claim 15, wherein the element density function and the element attributes evaluation include at least one of:

(i) forming a graphical representation of a transistor structure; and

(ii) forming a graphical representation of a latchup structure.

[c21] 21. A method comprising the steps of:

forming a layout representation in a function block;

defining a mathematical graph representation of latchup parasitic in the function block;

providing a latchup density function from the mathematical graph representation; and

placing the function block in a semiconductor chip to minimize latchup based on the latchup density function.

[c22] 22. The method as recited in claim 21, wherein the placement of the function block is associated with an injection source.

[c23] 23. The method as recited in claim 21, wherein a form factor of the function block is formed to minimize latchup sensitivity.

[c24] 24. A method comprising the steps of:
identifying injection source and elements associated with the at least one functional circuit block;
evaluating global latchup of injector to functional circuit block distance and functional circuit block latchup;
evaluating form factors and placement of the functional circuit block; and
determining whether there is a sufficient cost factor savings based on the form factors and placement of the functional circuit blocks, if not,
modifying placement of the functional circuit block relative to other functional circuit blocks based on an element density function.

[c25] 25. An apparatus comprising:
a circuit schematic representation of a at least one type of transistor;

a circuit schematic representation of at least one type of structure;

a design system which defines the circuit schematic representation of the at least one type of transistor and one type of structure;

a design system to evaluate a circuit density and attributes of the at least one type of transistor and one type of structure; and

a design system that places functional blocks based on latchup density functionals based on the evaluation of the circuit density and attributes.

[c26] 26. The apparatus of claim 25, wherein the at least one type of transistor is an npn and pnp transistor and the one type of structure is at least a pnpn structure.

[c27] 27. A computer program product comprising:

a computer usable medium having computer readable program code embodied in the medium, the computer program product having:

computer program for identifying element density of at least one functional circuit block;

computer program for identifying element attributes of elements associated with the at least one functional circuit block;

computer program for forming an element density function parameterized from the element attributes;

and

computer program for modifying placement of the at least one functional circuit block relative to other functional circuit blocks based on the element density function to substantially eliminate latching effects in a circuit.